**IN THE CLAIMS:**

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

an MISFET, which is provided on the semiconductor substrate and includes a gate insulating film, a gate electrode and source/drain regions;

a ferroelectric FET, which is provided on the semiconductor substrate and includes a ferroelectric film provided over the semiconductor substrate, a control gate electrode provided on the ferroelectric film and source/drain regions;

a memory circuit block, in which the ferroelectric FET is arranged; ~~and~~

a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block; and

a logic circuit block, in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block.

2. (Original) The device of claim 1, wherein the ferroelectric FET further includes:

a gate insulating film provided on a part of the substrate, which part is located between the source/drain regions of the ferroelectric FET;

a gate electrode provided on the gate insulating film of the ferroelectric FET;

an interlevel dielectric film covering at least the gate electrode of the ferroelectric FET;

an intermediate electrode provided on the interlevel dielectric film; and

a contact member connecting the intermediate electrode and the gate electrode of the ferroelectric FET together; and

wherein the ferroelectric film is provided on the intermediate electrode.

3. (Original) The device of claim 2, wherein the gate electrode of the ferroelectric FET and the gate electrode of the MISFET are formed out of the same conductor film.

4. (Original) The device of Claim 2, further comprising: a first interconnect connected to the intermediate electrode; and a second interconnect connected to the control gate electrode, and

wherein polarization is created in the ferroelectric film with a voltage applied between the first and the second interconnects.

5. (Cancelled).

6. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

a) forming a gate insulating film and a gate electrode for each of first- and second-channel-type MISFETs and a ferroelectric FET over a semiconductor substrate;

b) implanting ions of a dopant for forming source/drain regions from over the gate electrode of the ferroelectric FET and the gate electrode of one of the first- and second-channel-type MISFETs;

c) implanting ions of another dopant for forming source/drain regions from over the gate electrode of the other MISFET;

d) forming an interlevel dielectric film covering the gate electrodes of the MISFETs and the ferroelectric FET, forming a contact hole, which passes through the interlevel dielectric to reach the gate electrode of the ferroelectric FET, and then filling the contact hole with a conductor material to form a contact member;

e) forming an intermediate electrode, a ferroelectric film and a control gate electrode over the interlevel dielectric film so that the intermediate electrode is connected to the contact member and that the ferroelectric film is in contact with an upper surface of the intermediate electrode and that the control gate electrode faces the intermediate electrode with the ferroelectric film interposed therebetween;

f) forming a memory circuit block, in which the ferroelectric FET is arranged; ~~and~~

g) forming a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block; and

h) forming a logic circuit block, in which the MISFET is arranged, including a processor for transferring data do and from the memory circuit block.

7. (Currently Amended) The method of claim 6, further comprising the steps of:

~~h)~~ i) forming an upper-level dielectric film on the interlevel dielectric film after the step e) has been performed;

~~i)~~ j) forming two contact holes which pass through the upper-level dielectric film to reach the intermediate and control gate electrodes of the ferroelectric FET, respectively, and then filling the contact holes with a conductor material to form first and second contact members, which make electrical contact with the intermediate and control gate electrodes, respectively; and

~~j)~~ k) forming first and second interconnects, which are connected to the first and second contact members, respectively, on the upper-level dielectric film.